AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (previously presented): A level converting circuit for converting a signal level of a first logic circuit to which a first power source is supplied into a signal level of a second logic circuit to which a second power source is supplied, characterized by including

a pull-up and/or pull-down circuit in which the second power source is supplied to a level conversion output of a level conversion core circuit and a switching circuit between a GND power source terminal (ground power source terminal) of the level conversion core circuit and a GND power source (ground power source), the switching circuit being controlled by a third logic circuit to produce a control signal under control of the first power source,

the third logic circuit producing control signals to control the pull-up and/or pull-down circuit and the switching circuit,

the level conversion core circuit including a p-MOS cross-coupled latch including at least two first p-MOS, a differential n-MOS including at least two n-MOS, and at least two second p-MOS,

the p-MOS cross-coupled latch including a source terminal connected to the second power source and a gate terminal connected to a level conversion output which is each drain terminal of a second pMOS,

the differential n-MOS including each source terminal connected to the GND power source, each drain terminal connected to the level conversion output, and each gate terminal connected to a level conversion input,

the second p-MOS including each source terminal connected of the first p-MOS, each gate terminal connected to the level conversion input, and each drain terminal connected to the level conversion output.

2. (previously presented): A level converting circuit for converting a signal level of a first logic circuit to which a first power source is supplied into a signal level of a second logic circuit to which a second power source is supplied, characterized by including

a switching circuit between a power source terminal of a level conversion core circuit and the second power source, the switching circuit being controlled by a third logic circuit which generates a control signal under control of the first power source, and a pull-up and/or pull-down circuit at an output of the level conversion core circuit, the pull-up and/or pull-down circuit being controlled by the third logic circuit,

the third logic circuit producing control signals to control the pull-up and/or pull-down circuit and the level conversion core circuit.

3. (original): A level converting circuit in accordance with claim 1 or 2, characterized in that:

the level conversion core circuit includes a p-MOS cross-coupled latch including at least two p-MOS and a differential n-MOS including at least two n-MOS;

each of the p-MOS includes a source terminal connected to the second power source terminal and a gate terminal connected to a level conversion output which is each drain terminal; and

each of the n- MOS includes a source terminal connected to the cross-coupled latch and the GND power source terminal, a drain terminal connected to the level conversion output, and a gate terminal connected to a level conversion input.

4. (canceled).

5. (previously presented): A level converting circuit for converting a signal level of a first logic circuit to which a first power source is supplied into a signal level of a second logic circuit to which a second power source is supplied, characterized by including

a pull-up and/or pull-down circuit in which the second power source is supplied to a level conversion output of a level conversion core circuit and a switching circuit which is disposed between a power source terminal of the level conversion core circuit and the second power source and which is controlled by a third logic circuit, the third logic circuit generating a control signal under control of a first power source, wherein the control circuit is controlled by a control signal from the third logic circuit.

6. (original): A level converting circuit for converting a signal level of a first logic circuit to which a first power source is supplied into a signal level of a second logic circuit to which a second power source is supplied, characterized by including

a pull-up and/or pull-down circuit in which the second power source is supplied to a level conversion output of a level conversion core circuit, a control circuit to which the second power source is supplied and which receives as inputs thereto a level conversion input signal and the level conversion output signal, and a switching circuit which is disposed between a power source terminal of the level conversion core circuit and the second power source and which is controlled by a third 'logic circuit, the third to circuit generating a control signal under control of the first power source, wherein the control circuit is controlled by a control signal from the third 'logic circuit.

7. (previously presented): A level converting circuit, characterized in that the third logic circuit controls the control circuit by a control signal from the third logic circuit, and the control circuit produces control signals to control the pull-up and/or pull-down circuit and the level conversion core circuit.

8. (original): A level converting circuit in accordance with claim 7. characterized in that the control circuit further produces

a control signal to control the pull-up and/or pull-down circuit to thereby control the pull-up and/or pull-down circuit.

9. (canceled).

10. (previously presented): A level converting circuit in accordance with claim 8, characterized in that the pull-up and/or pull-down circuit comprises a p-MOS including a source terminal connected to the second power source, a gate terminal connected to a control signal, and a drain terminal connected to one of the level conversion outputs and an n-MOS including a source terminal connected to a GND power source, a gate terminal connected to an inverted signal of a control signal, and a drain terminal connected to other one of the level conversion outputs.

11. (previously presented): A level converting circuit in accordance with claim 7, characterized in that the pull-up and/or pull-down circuit includes at least two p-MOS each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, each drain terminal of other pMOS being connected to each of the level conversion outputs; at least two n-MOS each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level conversion outputs, and additionally at least two p-MOS each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the third logic circuit, a drain terminal of other p-MOS being connected to each of the level conversion outputs.

12. (previously presented): A level converting circuit in accordance with claim 7, characterized in that the pull-up and/or pull-down circuit includes at least two p-MOS each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, each drain terminal of other p

MOS being connected to each of the level conversion outputs; at least two n-MOS each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level conversion outputs; and additionally a p-MOS including a source terminal connected to the second power source, a gate terminal connected to a control signal from the third logic circuit, a drain terminal connected to one of the level conversion outputs.

13. (previously presented): A level converting circuit in accordance with claim 7, characterized in that the pull-up and/or pull-down circuit includes at least two p-MOS each of which includes a source terminal connected to the second power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to each of the level conversion outputs, at least two n-MOS each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level conversion outputs: additionally a p-MO including a source terminal connected to the second power source, a gate terminal connected to a control signal from the third logic circuit, and a drain terminal connected to one of the level conversion outputs; and additionally an n-M-ZOS including a source terminal connected to the

GND power source, a gate terminal connected to a control signal from the third logic circuit or to an inverted signal of the control signal, and a drain terminal connected to other one of the level conversion outputs.

14. (previously presented): A level converting circuit in accordance with claim 7, characterized in that the pull-up and/or pull-down circuit includes at least two p-MOS each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, a drain terminal of other pMOS being connected to each of the level conversion outputs; at least two n-MOS each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level conversion outputs; and additionally an n-MOS including a source terminal connected to the GND power source, a gate terminal connected to a control signal from the third logic circuit or to an inverted signal of the control signal, and a drain terminal connected to one of the level conversion outputs.

15. (previously presented): A level converting circuit in accordance with claim 7, characterized in that the control circuit comprises a NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output signal, a positively inverted signal of the level conversion output signal, and a control output of the third logic circuit, wherein an output signal of the NAND circuit is produced to control a signal.

16. (previously presented): A level converting circuit in accordance with claim 15, characterized in that the NAND circuit is of a CMOS circuit configuration and the p-MOS transistor to which the level conversion input signal is connected includes a transistor at least having a small ratio of a channel width/a channel length or a high threshold value.

17. (previously presented): A level converting circuit in accordance with claim 15, characterized in that the NAND circuit is of a CMOS circuit configuration and the n-MOS transistor to which a control signal output of the third logic circuit is connected includes a source terminal connected to a GND power source.

18. (canceled).

19. (original): A level converting circuit in accordance with claim 15, characterized in that the pull-up and/or pull-down circuit further includes at least two p-MOS each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, a drain terminal of other pMOS being connected to each of the level conversion outputs; and additionally at least two p-MOS each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the third logic circuit, a drain terminal of other p-MOS being connected to each of the level conversion outputs.

20. (original): A level converting circuit in accordance with claim 15, characterized in that the pull-up and/or pull-down circuit further includes at least two p-MOS each of which includes a source terminal connected to the second power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to each of the level conversion outputs; and additionally a p-MOS including a source terminal connected to the second power source, a gate terminal connected to a control signal from the third logic circuit, and a drain terminal connected to one of the level conversion outputs.

21. (original): A level converting circuit in accordance with claim 15, characterized in that the pull-up and/or pull-down circuit includes at least two p-NIOS each of which includes a source terminal connected to the second power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to each of the level conversion outputs: additionally a p-MOS including a source terminal connected to the second power source, a gate terminal connected to a control signal from the third logic circuit, and a drain terminal connected to one of the level conversion outputs; and

additionally an n-MOS including a source terminal connected to the GND power source, a gate terminal connected to a control signal from the third logic circuit or to an inverted signal of the control signal, and a drain terminal connected to other one of the level conversion outputs.

22. (original): A level shifter in accordance with claim 18, characterized in that the pull-up and/or pull-down circuit includes at least two p-MOSs each of which includes a source

terminal connected to the second power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to each of the level shift outputs; and additionally an n-MOS including a source terminal connected to the GND power source, a gate terminal connected to a control signal from the third logic circuit or an inverted signal of the control signal, and a drain terminal connected to one of the level shift outputs.

23. (original): A level shifter in accordance with claim 7, characterized in that the control circuit comprises a NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit, a NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output, and a control output of the third logic circuit, and at least two inverters to which the second power source is supplied and which respectively receive as inputs thereto outputs from the NAND circuits, wherein each output signal from the inverters is produced as a control signal.

24. (original): A level shifter in accordance with claim 18, characterized in that the pull-up and/or pull-down circuit includes at least two n-MOSs each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level shift outputs and additionally at least two p-MOSs each of which includes a source terminal connected to the second power

source and a gate terminal connected to a control signal from the third logic circuit, a drain terminal of other p-MOS being connected to each of the level shift outputs.

25. (original): A level shifter in accordance with claim 23, characterized in that the pull-up and/or pull-down circuit includes at least two n-MOS each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level shift outputs and additionally a p-MOS including a source terminal connected to the second power source, a gate terminal connected to a control signal from the third logic circuit, and a drain terminal connected to one of the level shift outputs.

26. (original): A level shifter in accordance with claim 23, characterized in that the pull-up and/or pull-down circuit includes at least two n-MOSs each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level shift output; additionally a p-MOS including a source terminal connected to the second power source, a gate terminal connected to a control signal from the third logic circuit, and a drain terminal connected to one of the level shift outputs; and additionally an n-MOS including a source terminal connected to the GND power source, a gate terminal connected to a control signal from the third logic circuit or an inverted signal of the control signal, and a drain terminal connected to other one of the level shift outputs.

27. (original): A level shifter in accordance with claim 23, characterized in that the pull-up and/or pull-down circuit includes at least two n-MOSs each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level shift outputs and additionally an n-MOS including a source terminal connected to the GND power source, a gate terminal connected to a control signal from the third logic circuit or to an inverted signal of the control signal, and a drain terminal connected to other one of the level shift outputs.

28. (original): A level shifter in accordance with one of claims 14 to 17, characterized in that the control circuit comprises a NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output, a NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which respectively receive as inputs thereto outputs from the NOR circuits, wherein output signals respectively from the at least two NOR circuits and the at least two inverters are produced as control signals.

29. (original): A level shifter in accordance with claim 28, characterized in that the NOR circuits are of a CMOS circuit configuration and a p-MOS to which the level shift input signal is connected includes a transistor at least having a small ratio of a channel width/a channel length or a threshold value which is of a negative polarity and which is a large absolute value.

30. (original): A level shifter in accordance with claim 28, characterized in that the NOR circuits are of a CMOS circuit configuration and a control signal from the third logic circuit or an inverted signal thereof is connected to a p-MOS on a power source side.

31. (original): A level shifter in accordance with one of claims 19 to 22, characterized in that the control circuit comprises a NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output, a NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective NOR circuits, wherein each output signal from the inverters is produced as a control signal.

32. (original): A level shifter in accordance with one of claims 24 to 27, characterized in that the control circuit comprises a first NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output and a second NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, wherein each output signal from the first and second NOR circuits is produced as a control signal.

33. (original): A level shifter in accordance with claim 8, characterized in that the control circuit comprises an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output, a NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output, and a control output of the third logic circuit, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective NAND circuits, wherein output signals from the AND-NOR circuit, the NAND circuit, and the inverters are produced as control signals.

34. (original): A level shifter in accordance with claim 8 or 10, characterized in that the pull-up and/or pull-down circuit includes at least two p-MOSs each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, a drain terminal of other p-MOS being connected to each of the level shift outputs and at least two n-MOSs each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level shift outputs.

35. (original): A level shifter in accordance with claim 8, characterized in that the control circuit comprises an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output and a NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output, and a control output of the third logic circuit,

wherein respective output signals from the AND-NOR circuit and the NAND circuit are produced as control signals.

36. (original): A level shifter in accordance with claim 35, characterized in that the pull-up and/or pull-down circuit includes at least two p-MOSs each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal

from the control circuit, a drain terminal of other p-MOS being connected to each of the level shift outputs.

37. (original): A level shifter in accordance with claim 8, characterized in that the control circuit comprises an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output, a NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output, and a control output of the third logic circuit, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective NAND circuits, wherein each output signal from the inverters is produced as a control signal.

38. (original): A level shifter in accordance with claim 37, characterized in that the pull-up and/or pull-down circuit includes at least two n-MOSs each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level shift outputs.

39. (original): A level shifter in accordance with claim 34, characterized in that the control circuit comprises an OR-NAND circuit to which the second power source is supplied and

which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit, a NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the each of the NOR circuits, wherein each output signal from the OR-NAND circuit, the NOR circuits, and the inverters is produced as a control signal.

40. (original): A level shifter in accordance with claim 39, characterized in that the OR-NAND circuit is of a CMOS circuit configuration and a p-MOS to which the level shift input signal is connected has at least one condition that the p-MOS has a small ratio of a channel width/a channel length or a threshold value which is of a negative polarity and which is a large absolute value.

41. (original): A level shifter in accordance with claim 39, characterized in that the OR-NAND circuit is of a CMOS circuit configuration and a control signal from the third logic circuit is connected to an n-MOS on a GND power source side.

42. (original): A level shifter in accordance with claim 36, characterized in that the control circuit comprises an OR-NAND circuit to which the second power source is supplied and

which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit, a NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective NOR circuits, wherein each output signal from the inverters is produced as a control signal.

43. (original): A level shifter in accordance with claim 38, characterized in that the control circuit comprises an OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit and a NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, wherein each output signal from the OR-NAND circuit and the NOR circuit is produced as a control signal.

44. (original): A level shifter in accordance with claim 36, characterized in that the control circuit comprises an AND-NOR circuit to which the second power source is supplied and

which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output and an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, wherein each output signal from the AND-NOR circuits is produced as a control signal.

45. (original): A level shifter in accordance with claim 36, characterized in that the control circuit comprises an OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit, an OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective OR-NAND circuits, wherein each output signal from the inverters is produced as a control signal.

46. (original): A level shifter in accordance with claim 38, characterized in that the control circuit comprises an AND-NOR circuit to which the second power source is supplied and

which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output, an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective AND-NOR circuits, wherein each output signal from the inverters is produced as a control signal.

47. (original): A level converting circuit in accordance with claim 38, characterized in that the control circuit comprises an OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level conversion output signal, and a control output of the third logic circuit and an OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output, and a control output of the third logic circuit, wherein each output signal from the ORNAND circuits is produced as a control signal.

48. (previously presented): A level converting circuit in accordance with claim 47, characterized in that the level conversion core circuit comprises a p-MOS cross-coupled latch including at least two of the pMOS in which each source terminal is connected to the second

source and a gate terminal of other p-MOS is connected to each of the level conversion outputs, at least two p-NIOS switches including a source terminal connected to a drain terminal of the p-MOS, each gate terminal connected to a control signal from the control circuit, and each drain terminal connected to the level conversion outputs, and a differential n-MOS switch including at least two n-MOS each of which includes a source terminal connected to a GND power source, a drain terminal connected to the respective level conversion outputs, and a gate terminal connected to a level conversion input.

49. (currently amended): A level converting circuit in accordance with one of claims ~~11 to 14, 19 to 22, and 24 to 27~~ 11, 12, 13, 14, 19, 20, 21, 22, 24, 25, 26 or 27, characterized in that the control circuit comprises a first NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output signal. and a control output of the third logic circuit, a second NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level conversion output, and a control output of the third logic circuit, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective NAND circuits, wherein each output signal from the first and second NAND circuits and the at least two inverters is produced as a pull-up and/or pull-down control signal and each output signal of the inverters is produced as a control signal of the level conversion core circuit.

50. (currently amended): A level converting circuit in accordance with one of claims ~~11 to 14, 19 to 22, and 24 to 27~~11, 12, 13, 14, 19, 20, 21, 22, 24, 25, 26 or 27 characterized in that the control circuit comprises a NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level conversion output signal, and a control output of the third logic circuit or an inverted signal of the control output, a NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output, and a control output of the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which respectively receive as inputs thereto outputs from the respective NOR circuits, wherein each output signal from the NOR circuits and the inverters is produced as a pull-up and/or pull-down control signal and each output signal of the NOR circuits is produced as a control signal of the level conversion core circuit.

51. (canceled).

52. (original): A level shifter in accordance with claim 34, characterized in that the control circuit comprises an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit or an

inverted signal of the control output, a NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output, and a control output of the third logic circuit, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective NAND circuits, wherein each output signal from the AND-NOR circuit, the NAND circuit, and the at least two inverters is produced as a pull-up and/or pull-down control signal and each output signal of the inverters is produced as a control signal of the level shift core circuit.

53. (original): A level shifter in accordance with claim 39, characterized in that each output signal from the OR-NAND circuit, the NOR circuit, and the inverters is produced as a pull-up and/or pull-down control signal and each output signal of the OR-NAND circuit and the NOR circuit is produced as a control signal of the level shift core circuit.

54. (original): A level shifter in accordance with claim 8, characterized in that the control circuit comprises a first AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output, a second AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output, and a control output of the third logic

circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the first and second AND-NOR circuits, wherein each output signal from the first and second AND-NOR circuits is produced as a pull-up and/or pull-down control signal and each output signal of the inverters is produced as a control signal of the level shift core circuit, and the pull-up and/or pull-down circuit includes at least two p-MOSs each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, a drain terminal of other p-MOS being connected to each of the level shift outputs.

55. (original): A level shifter in accordance with claim 8, characterized in that the control circuit comprises a first OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit, a second OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the first and second OR-NAND circuits, wherein each output signal from the at least two inverters is produced as a pull-up and/or pull-down control signal and each output signal from the OR-NAND circuits is produced as a control signal of the level shift core circuit, and

the pull-up and/or pull-down circuit includes at least two p-MOSs each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, a drain terminal of other p-MOS being connected to each of the level shift outputs.

56. (previously presented): A level converting circuit in accordance with one of claims 5 to 8, characterized in that the control circuit comprises an AND-NOR circuit to which the second power source i s supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output signal, and a control output of the third logic circuit or an inverted signal of the control output, an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level conversion output, and a control output of the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective AND-NOR circuits. wherein each output signal from the inverters is produced as a pull-up and/or pull-down control signal, each output signal from the inverters is produced as a control signal of the level conversion core circuit, and

the pull-up and/or pull-down circuit includes at least two n-MOS each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level conversion outputs.

57. (previously presented): A level converting circuit in accordance with one of claims 5 to 8, characterized in that the control circuit comprises a first OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level conversion output signal, and a control output of the third logic circuit and a second OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output, and a control output of the third logic circuit, wherein each output signal from the first and second OR-NAND circuits is produced as a pull-up and/or pull-down control signal, each output signal from the OR-NAND circuits is produced as a control signal of the level conversion core circuit, and

the pull-up and/or pull-down circuit includes at least two n-VIOS each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level conversion outputs.

58. (previously presented): A level converting circuit in accordance with one of claims 5 to 8, characterized in that the control circuit comprises an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output signal, and a control output of the third logic circuit or an inverted signal of the control output, an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level

conversion output, and a control output of the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective AND-NOR circuits, wherein each output signal of the inverters is produced as a control signal of the level conversion core circuit.

59. (currently amended): A level converting circuit in accordance with one of claims ~~4 to 7 and 9 to 11~~5, 6, 7, 10, 11, 12, 13 or 14, characterized in that the control circuit comprises an OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level conversion output signal, and a control output of the third logic circuit and an OR-:`NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the i.evel conversion output, and a control output of the third logic circuit, wherein each output signal from the OR-NAND circuits is produced as a control signal of the level conversion core circuit.

60. (currently amended): A level converting circuit in accordance with one of claims ~~1, 3, 8, 58 and 59~~1 or 8, characterized in that:

the level conversion core circuit comprises a p-BIOS crosscoupled latch including at least two first p-MOS. a differential n-MOS including at least two n-MOS, and at least two second p-MOS, wherein:

the p-MOS cross-coupled latch includes a source terminal connected to the second power source and a gate terminal connected to a level conversion output which is each drain terminal of the second pMOS;

the differential n-MOS includes each source terminal connected to the GND power source, each drain terminal connected to the level conversion output, and each gate terminal connected to a level conversion input; and

the second p-MOS includes each source terminal connected of the first p-MOS, each gate terminal connected to the level conversion input, and each drain terminal connected to the 'level conversion output.

61. (original): A level converting circuit for converting a signal level of a first logic circuit to which a first power source is supplied into a signal level of a second logic circuit to which a second power source is supplied, characterized by including

a pull-down circuit at a level conversion output of a level conversion core circuit and a control circuit to which the second power source supplied and which receives as inputs thereto a level conversion input signal the level conversion output signal to produce control signals for a pull-down circuit and a level conversion core circuit, wherein the control circuit is also connected to control signals from the third logic circuit.

62. (original): A level converting circuit in accordance with claim 61, characterized in that the control circuit, the control circuit comprises a first OR-NAND circuit to which the

second power source is supplied and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level conversion output signal, and a control output of the third logic circuit and a second OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output, and a control output of the third logic circuit, wherein each output signal from the first and second OR-NAND circuits is produced as a pull-up and/or pull-down control signal, each output signal from the OR-NAND circuits is produced as a control signal of the level conversion core circuit, and

the pull-down circuit, the pull-up and/or pull-down circuit include at least two n-MOS each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level conversion outputs.

63. (original): A level converting circuit in accordance with claim 61, characterized in that the control circuit, the control circuit comprises a first OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level conversion output signal. and a control output of the third Logic circuit and a second OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output, and a control output of the third logic circuit or an inverted signal of the control output, wherein each

output signal from the first and second OR-NAND circuits is produced as a pull-up and/or pull-down control signal, each output signal from the OR-NAND circuits is produced as a control signal of the level conversion core circuit, and

the pull-down circuit, the pull-up and/or pull-down circuit include at least two n-MOS each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level conversion outputs.

64. (canceled).

65. (currently amended): A level shifter in accordance with one of claims ~~3, 5, 6, and 6~~1<u>5, 6 or 61</u>, characterized in that the control circuit comprises at least two NOR circuits to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit or an inverted signal of the control output and a NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output, and a control output of the third logic circuit or an inverted signal of the control output, wherein each output signal from the NOR circuits is produced as a control signal of the level shift core circuit.

66. (currently amended): A level shifter in accordance with one of claims ~~3, 11, 12, and 61~~11, 12, or 61, characterized in that the control circuit comprises at least two NAND circuits to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level shift input signal, an inverted signal of the level shift output signal, and a control output of the third logic circuit, a NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level shift input signal, a positively inverted signal of the level shift output signal, and a control output of the third logic circuit, and at least two inverters to which the second power source is supplied and which receives as inputs thereto outputs from the respective NAND circuits, wherein each output signal from the inverters is produced as a control signal of the level shift core circuit.